Turning now to the drawings, Figure 1 shows a schematic representation of a semiconductor structure 10 that incorporates a preferred embodiment of this invention. The semiconductor structure 10 is a portion of a three-dimensional, field-programmable, write-once memory array of the general type described in co-pending U.S. Patent Application Serial No. 09/928,536, filed on the same day as the present application and hereby incorporated by reference in its entirety. The portion of the memory array shown in Figure 1 includes layers 12, 14, 16 18, and 19 that are patterned with a line width of 0.25 μm. The layer 14 acts as a low-resistivity conductor, and can for example correspond to a word line in a memory array. The layer 19 acts as a dielectric rupture anti-fuse layer, and the layer 18 operates as a diode component. The layers 14, 22 are electrical contacts to the adjacent diode components as well as contacts to the outside world.

IN THE CLAIMS

Please amend Claims 2-6 and 8 as follows. Appendix B (at Tab B) contains a marked-up version of those claims showing the changes being made.

2. (Amended) The semiconductor structure of Claim 1 wherein $t1 \geq 2.2t2$.

3. (Amended) The semiconductor structure of Claim 1 wherein $t1 = 2.3t2, \pm 0.1t2$.

4. (Amended) The semiconductor structure of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.